

Power Quality Improvement by 11 Level Multilevel Inverter with Reduced Number of Switches

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Abstract: This paper deals with 11-level multilevel inverter. Almost all the drawbacks of the conventional multilevel inverters is rectified by the proposed topology. This topology uses less number of switches as compared with conventional topology, where it reduces the complexity and overall size of the system which in turn reduces the harmonics and cost of the entire system. Fewer switches will be conducting for specific time intervals so switching loss is also reduced in the proposed topology. A 11-level inverter simulation is carried with the implementation of nearest level control. The proposal is validated by extensive simulation studies.

Index Terms: multilevel inverter, cascaded multilevel inverter, Total Harmonic Distortion (THD).

INTRODUCTION

Multilevel inverters are considered today as the state-of-the-art power-conversion systems for high-power and power-quality demanding applications. Multilevel inverters are currently considered as a better industrial solution for high dynamic performance and power-quality demanding applications, covering a wide power range. The increase of the world energy demand has entailed the appearance of new power converter topologies and new semiconductor technologies.

Highly popular voltage-source multilevel inverters, which can be divided into three categories, that's are neutral point clamped (NPC), flying capacitor (FLC), and cascade H-bridge. Cascaded H-bridge multilevel inverter has been researched for high voltage applications since it has advantages in number of components, high reliability, and modularity. This inverter can avoid extra clamping diodes or voltage balancing capacitors [11], [9]. A single phase m-level configuration of the cascaded multilevel inverter shown in the Fig.1. One of the demerits of cascade multilevel inverter is that as the number of levels increases, the number of H-bridges also increases [14]. This makes the modulation strategy more complex. Depending upon the voltage source used, Cascaded multilevel inverter are classified into two that's are symmetrical and asymmetrical Cascaded multilevel inverter [6]. In asymmetrical Cascaded multilevel inverter dc voltages are in different proportion. So the Inverters can be designed with different switch technologies. To reduce the number of DC sources in a symmetrical cascaded topology DC sources are replaced by the capacitors. It may cause voltage balancing problem [7], [12].

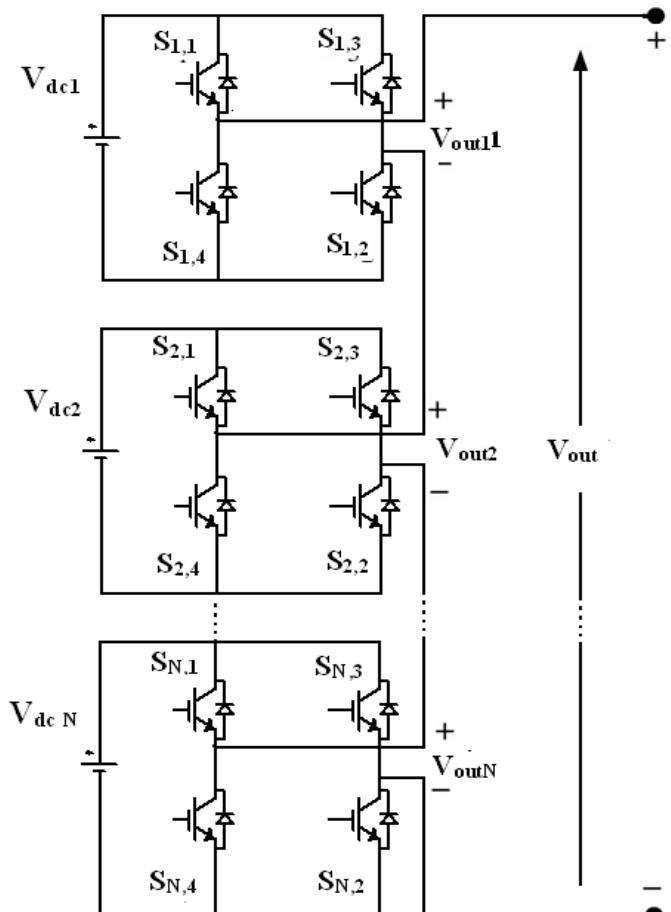


Fig.1.conventional cascaded multilevel inverter

The number of high-frequency switches is increased in Reverse voltage (RV) topology, hence reliability of the converter is decreased and the switching loss is also more [1]. This paper presents a hybrid multilevel inverter, the suggested topology requires less number of components as compared to conventional topologies. Hence it reduces the installation area, gate drivers needed, and consequently the cost of the whole setup[8]. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. [14]. Nearest level control is utilized to drive the multilevel inverter and can be extended to any number of levels.

voltage levels. The simulation results of the proposed topology are also presented.

DVR BASIC CONFIGURATION

The proposed multilevel topology is a hybrid multilevel inverter. Fig.2. shows the basic block diagram. The proposed system consists of a normal H bridge inverter and some auxiliary switches. In auxiliary switching part consisting of set series connected smaller multilevel inverter blocks. In this reduced switching topology separates the output of the multilevel inverter into two parts. One part is named level generation part and it is responsible for level generating in positive polarity. The other part is called polarity generation part. The H-bridge is responsible for generating the polarity of the output voltage. H-bridge consisting of four switches and these switches are operating at fundamental frequency. The proposed eleven levels inverter is shown in Fig. 3. As can be seen, it requires 12 switches and five isolated sources. The main idea of this proposed topology as a multilevel inverter is that the left side in Fig. 3 generates the required output levels (without polarity) and the right side of the circuit (H-bridge inverter) decides about the polarity of the output voltage.

General Description

The proposed system consists of a normal H bridge inverter and some auxiliary switches. A stepped waveform is generated at the output according to how the sources are being connected to the load. The H Bridge is operated normally to generate alternating voltage output. During positive half cycle, switches M1 and M2 are turned on and the level selecting switches are operated to get different voltage levels. To generate the negative half cycle, switches M3 and M4 are conducting while the level selecting switches are operated to get a staircase voltage at the output. To obtain the first level, the dc source V1 must be connected to the load. To generate the second level, both V1 and V2 must be connected to the load. The rest of the sources are also connected in steps to the load in similar manner. The switches are controlled in such a way that respective sources are connected to the load during desired time intervals.

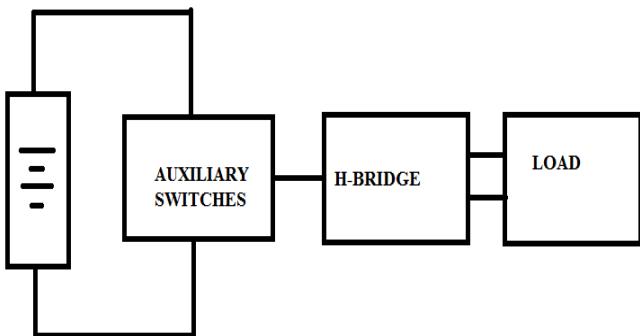


Fig .2. Block diagram

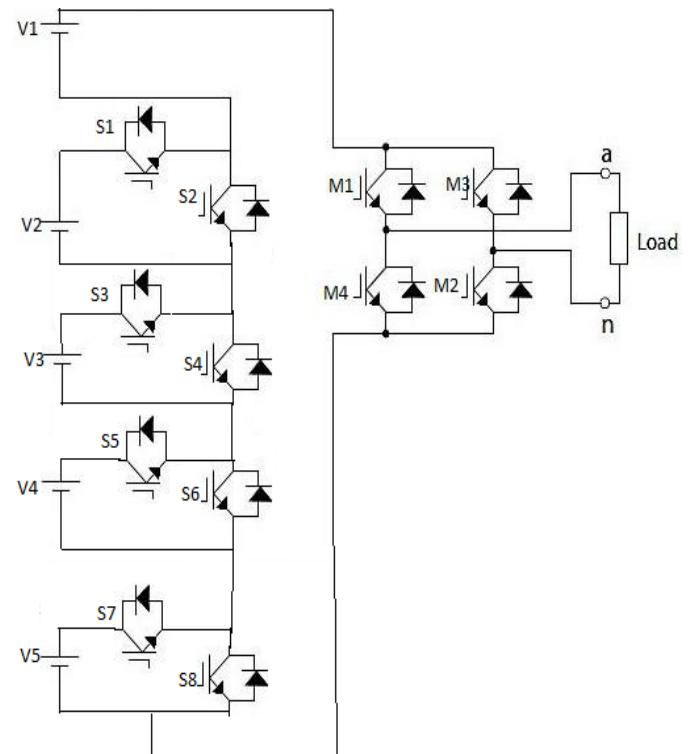


Fig.3. proposed multilevel inverter

In the proposed topology the total switch count is 12 for a eleven level multilevel inverter, in case of a conventional cascaded multilevel inverter it would be 20. Number of switches and gate driver circuits reduced in this topology so reducing the complexity of the overall circuit. It reduces the installation area and consequently the cost of the whole setup.

SWITCHING SEQUENCE

Va	S1	S2	S3	S4	S5	S6	S7	S8
Vdc	ON	ON	ON	ON	OFF	OFF	OFF	OFF
2Vdc	OFF	ON	ON	ON	ON	OFF	OFF	OFF
3Vdc	OFF	OFF	ON	ON	ON	ON	OFF	OFF
4Vdc	OFF	OFF	OFF	ON	ON	ON	ON	OFF
5Vdc	OFF	OFF	OFF	OFF	ON	ON	ON	ON

Switching Sequence

Switching sequences in the proposed multilevel inverter are simpler as compared to conventional topologies. There is no need to control negative cycle so it does not generate negative pulses. Thus, there is no need for extra conditions for controlling the negative voltage. In Table.1. shows the switching sequence of the proposed topology. In this, the switching transition is minimum during each mode transfer so there is a reduction in the switching loss. Switches(S1-S8) are the level selection switches and switching pulses corresponding to each switches are shown in fig.4.

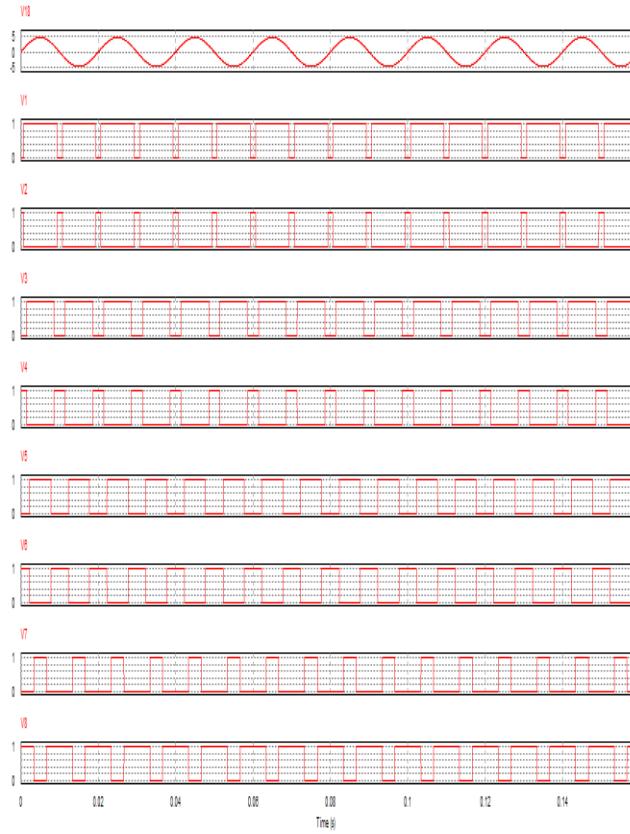


Fig .4. Switching Pulses

PWM TECHNIQUE

PWM Techniques has been extensively put to use in multilevel inverters. Instead of PWM method a simple control logic is used. In multiple carrier method for an m level inverter $m-1$ carriers are needed [2]-[5]. It can be seen from a sine wave that it takes different durations if it is moving from one voltage level to another voltage level from Fig.4. So a sine wave is taken and checked whether its amplitude is in between two adjacent voltage levels [13]. If so, the corresponding source is connected to the load and in similar way it is proceeded until all the source voltages are connected to load. The duration of different levels at the output changes each time, when the sine wave amplitude changes from one desired level to another, which makes the staircase output much more similar to a sine wave.

SIMULATION RESULTS

The simulation case study has been carried out software to validate the result. Fig.6. Shows the simulation model of the proposed topology. To generate the 11- level output voltage, 12 IGBTs and five DC power source of 24 Volts are used. Pulses are generated by using nearest level control method. The simulated Output voltage is shown in Fig.7. and the harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink.

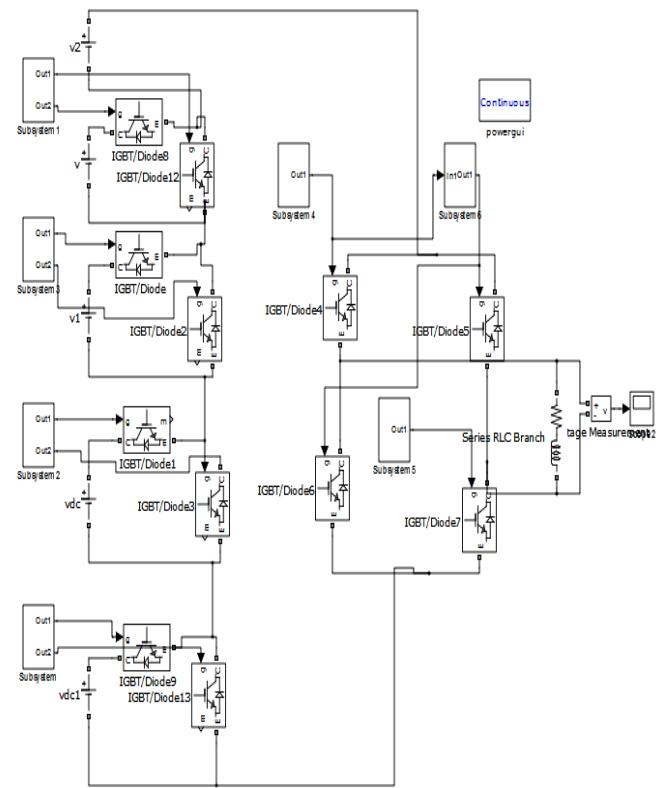


Fig.6.Simulation model of the proposed inverter

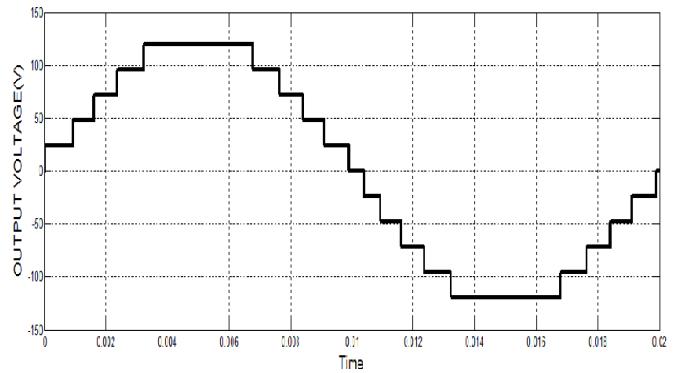


Fig.7. Output voltage of proposed inverter

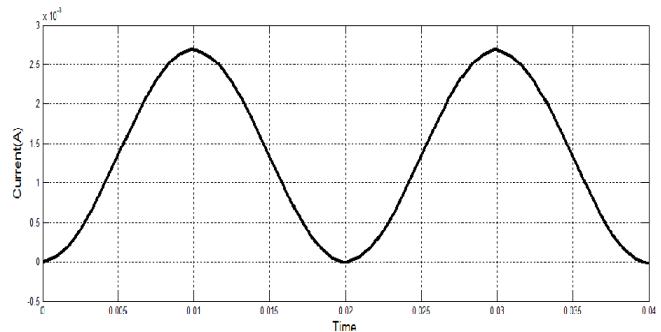


Fig.8. Current Waveform of the proposed inverter

The 11 level inverter output is shown in Fig.7. It has 11 levels of voltages in a half cycle and because of the unequal step widths, it resembles much more to a sine wave. As a result, the harmonic spectrum of the output will be improved. Current waveform of the inverter output is shown in Fig.8. Since the load is inductive, the load current will lag behind the load voltage waveform. The FFT analysis of the output voltage waveform must be carried out to find the THD of the output voltage waveform.

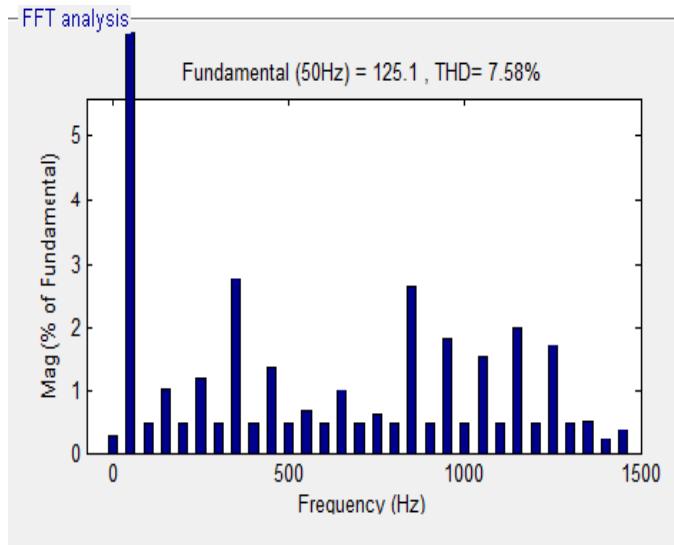


Fig.9. FFT analysis of output voltage with nearest level control

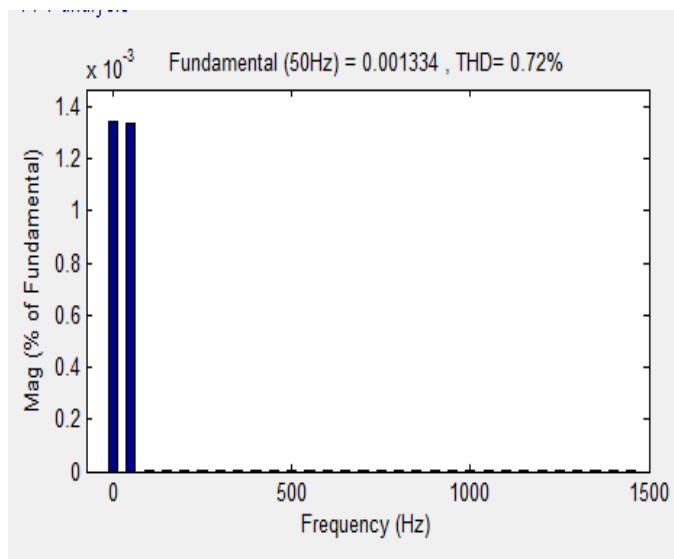


Fig.10. FFT analysis of output current with nearest level control

Total harmonic distortion (THD) of the proposed topology is 7.58% without using the LC filter is shown in Fig.8. FFT analysis of output current waveform is shown in Fig.10. The resulting current THD was .72%, which complies with the IEEE 519 harmonic standard.

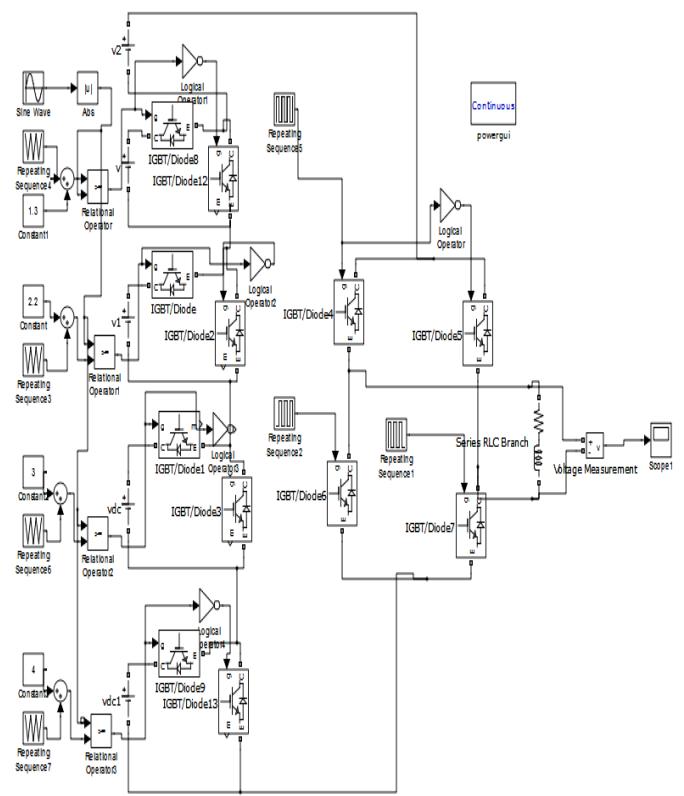


Fig.11. simulation model of proposed inverter with multicarrier PWM method

The Fig.11. shows the simulated model of the proposed 11-level multilevel inverter topology with conventional multicarrier PWM method. A carrier frequency of 5 kHz is generated and compared with a reference sine wave of 50 Hz. Its output voltage waveform and FFT analysis is also shown in Fig.12. and in Fig.13.

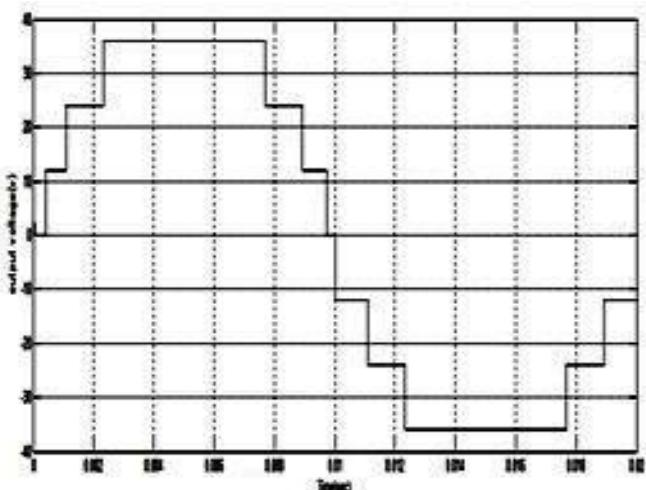


Fig.12. output voltage waveform of the proposed inverter with multicarrier PWM method

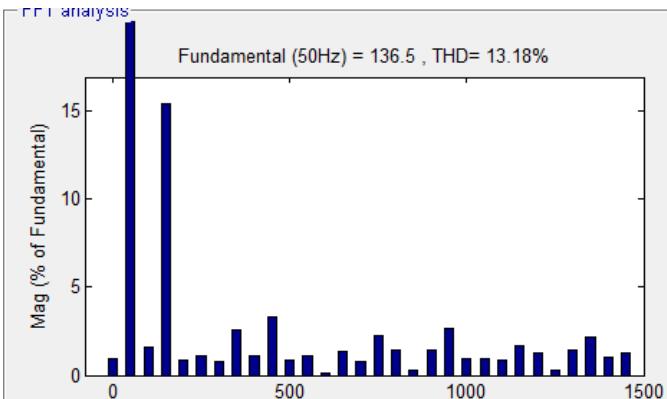


Fig.13. FFT analysis of output voltage with multicarrier PWM method

Total harmonic distortion (THD) of the proposed topology with multiple carrier method is 13.18%. By comparing Fig.9. and Fig.13. It can be seen that nearest level control method is better than multiple carrier method .

COMPARISON WITH CONVENTIONAL TOPOLOGY

Compared to other topologies the proposed topology has many advantages. It does not have any voltage unbalancing problems as in flying capacitor type topology. It has much more reduced no of switches compared to cascaded topology. A single H bridge can generate 3 voltage levels: +Vdc,0, -Vdc. Table.2. shows the comparison with conventional cascaded multilevel inverter with proposed system.

COMPARISON WITH CONVENTIONAL TOPOLOGY

	No. of Levels	No. of Switches
Cascaded Multilevel Inverter	11	20
Proposed Multilevel Inverter	11	12

CONCLUSION

A single phase eleven level cascaded multilevel inverter topology has been shown to produce an increased stepped output with less number of semiconductor switches. With fewer switches, controlling the overall circuit becomes less complex, the size and installation area are reduced. Switching loss and THD are reduced as compared to conventional topologies. Instead of conventional PWM method nearest level control method is used so that control parts become simple. The proposed circuit is performing harmonic reduction with reduced no of switches. Simulation results using MATLAB is also provided to validate the design.

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